UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/390,079	09/03/1999	DARREN KERR	112025-0167	6305

24267 7590 06/27/2003

CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER
ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
2183	15

DATE MAILED: 06/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/390,079	Kerr et al.
Examiner	**Group Art Unit**
Richard Ellis	2183

–The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address–

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on January 28, 2003.

☐ This action is FINAL

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-21 and 28-53. is/are pending in the application.

☐ Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-21 and 28-53. is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

1. The request filed on January 28, 2003 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/390,079 is acceptable and a CPA has been established. An action on the CPA follows.

2. Claims 1-21 and 28-37 remain for examination. Claims 38-53 are newly presented for examination.

3. The drawings are objected to under 37 CFR § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" claimed in claim 45 must be shown or the feature canceled from the claim. No new matter should be entered.

4. Applicant is required to submit a proposed drawing correction in response to this Office Action. Any proposal by the applicant for amendment of the drawings to cure defects must consist of two parts:

   a) A *separate* letter to the Draftsman in accordance with MPEP § 608.02(r); and,

   b) A print or pen-and-ink sketch showing changes in *red ink* in accordance with MPEP § 608.02(v).

5. The following in a quotation of the first paragraph of 35 USC 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 45 is rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" of claim 45 is not described within the specification, therefore, because it is not described, it is impossible that the inventors had possession of the claimed invention at the time of filing.

7. Claim 45 is rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" is not described in the specification or drawings. Therefore, due to lack of

description, it is not possible for the specification to enable one skilled in the art to make and/or use the invention.

8. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The claimed limitation of "micro-opcodes to initiate memory prefetches without requiring a dedicated instruction" present in new claim 45 does not exist within the specification.

9. Claims 46-51 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A) The scope of meaning of the following terms are unclear:

1. "specifies one of" claim 46; This claim contains the phrase "specifies one of" without reciting a set of two or more items from which to select "one of" from. It appears that the words "one of" should be deleted from the claim to remove any ambiguity as to whether the claim intended to claim a single item, or one item selected from a set of possible items. Claims 47-51 inherit the ambiguity from their parent claim 46.

10. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a)shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

12. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

13. Claims 1-21 are rejected under 35 USC 102(e) as being clearly anticipated by Asato, U.S. Patent 6,145,074.

14. Claims 36-37 and new claims 52-53 (when dependent upon claim 9) are rejected under

35 USC § 103 as being unpatentable over Asato, U.S. Patent 6,145,074.

Asato was cited as a prior art reference in paper number 12, mailed November 18, 2002.

15. The rejections of claims 1-21 and 36-37 are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 12, mailed November 18, 2002. Rejections for claims 52-53 (when dependent upon claim 9) appear below.

16. New claims 38-39 are rejected under 35 USC 102(e) as being clearly anticipated by Asato, U.S. Patent 6,145,074.

17. As to claim 38, Asato taught a pipeline (2) containing instruction decode, writeback and execution stages (applicant has simply claimed the inherent definition of a pipeline, in addition Asato at fig. 16 shows that he is aware that applicant's claimed components are the prior art definition of a pipeline, see the D, E1, E2, and W stages, D standing for decode, E1 and E2 for execution, and W for writeback), wherein the execution stage has multiple parallel execution units including a current execution unit and an alternate execution unit (fig. 6, 21-1 ... 21-4); and,

explicitly controlling data flow within the pipeline stages of the processor through the use of a register result bypass (RIRB) operand (fig. 1, b1, b2, fig. 5, b1, b2, p1, p2) to bypass the writeback stage and to allow result data from an alternate execution unit (fig. 6, 21-1 ... 21-4) to flow directly to an input execution register (fig. 2, bp1, bp2, 9, 10, 5, 6, 3, 4, fig. 7, "To pipeline register 3", "From 21-1 ... 21-4").

18. As to claim 39, Asato taught that the RIRB operand (fig. 5, b1, b2, p1, p2) explicitly infers feedback of the data delivered from an alternate one of the execution units ("From 21-1 ... 21-4) to an input register of the current execution unit ("To pipeline register 3") over a feedback path (212).

19. Claims 28-35, new claims 40-51, and new claims 52-53 (when dependent upon claim 46) are rejected under 35 USC § 103 as being unpatentable over Nakada, U.S. patent 5,638,526, in view of Asato, U.S. Patent 6,145,074.

Nakada taught (e.g. see figs. 1(a)-15) the invention substantially as claimed (as per claim 40), including a data processing ("DP") system comprising:

A) a pipeline of a processor (fig. 4) the pipeline having a plurality of stages including

instruction decode, writeback, and execution stages (applicant has claimed the inherent stages present in a computer pipeline), the execution stage having a plurality of parallel execution units (fig. 4, ALU1, ALU2);

B) a multiplexer connecting parallel execution units (SEL11 ... SEL22);

C) an instruction set of the processor (col. 1 lines 65-67), the pipeline providing for bypassing of a source operand from a previous instruction executing in a pipeline stage of the processor to the source operand of a current instruction [source operand bypassing] (fig. 4, SEL11, OP11, SEL21, OP21, col. 4 lines 4-45).

20. Nakada did not teach that the instruction set defined a register decode value that controlled the multiplexer to control the bypassing functionality. However, Asato taught a system whereby the instruction set of the processor defined register decode values (fig. 1, b1, b2, fig. 5, b1, b2, p1, p2) which were utilized to directly control bypassing functionality within Asato's system (col. 2 lines 47-58). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have modified Nakada's bypassing network to be controlled by register decode values contained in instructions as taught by Asato because Asato taught that placement of register decode values into the instructions for control of the bypassing network provided advantages of reduced hardware, shorter processor design cycles, and shorter design correctness verification cycles (col. 2 lines 53-62).

21. As to claim 41, Nakada taught a register file containing a plurality of general-purpose registers for storing intermediate result data processed by the execution units (fig. 4, REG).

22. As to claim 42, Nakada taught a memory for storing one of transient data unique to a specific process and pointers referencing data structures (in other words a "main memory" which is inherently present in all computers).

23. As to claim 43, Nakada in view of Asato taught a source bypass operand (RISB) that allows source operand data to be shared among the parallel execution units of the pipelined processor (Nakada fig. 4, OP11, SEL11, SEL12, OP21, SEL21, SE22, Asato fig. 5, b1, b2, p1, p2).

24. As to claim 44, Nakada taught a main execution unit (ALU1) and a secondary execution unit (ALU2), wherein the RISB operand allows the second execution unit (ALU2) to receive data (OP11, SEL21, SEL22) stored at a memory address specified by a displacement

operand in the previous instruction executed by the main execution unit (col. 2 lines 30-39).

25. As to claim 45, Nakada taught an opcode directed to the main execution unit (OP1, R11, R12), the opcode having sufficient bits to encode a displacement operand (col. 3 lines 46-52); and,

an opcode directed to the secondary execution unit (OP2, R21, R22).

26. Nakada combined with Asato did not teach a micro-opcode for initiating memory prefetches without requiring a dedicated instruction. However, because applicant's specification provides no support or teaching for this "micro-opcode" it can only be interpreted as the literal meaning of the words in the claim. As such, this is simply a traditional well known prefetch request to cache or memory by a processor and official notice of such is hereby taken. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have included a prefetch operation because of the well known advantages of prefetching providing for reducing memory latency by beginning an access sooner than it otherwise would have happened.

27. As to new claims 46-51, they do not teach or define above the invention claimed in claims 40-45 and are therefore rejected under Nakada in view of Asato for the same reasons set fourth in the rejection of claims 40-45, supra.

28. As to new claim 50, Nakada taught realizing two memory references through the use of a single bus operation over a local bus (fig. 4, OP11 stores a previous memory reference (read from REG), local bus RCPS1 reuses the value stored in OP11 as source input for another instruction, thereby not requiring the cached value in OP11 to be read out of memory a second time, see col. 2 lines 50-62).

29. As to claim 51, Asato taught that the RISB operand was encoded with fewer bits than those needed for a full displacement address (fig. 5, note narrower width of space for b1, b2, p1, p2, vs. the s1, s2, and dst fields).

30. As to claims 28-35, they do not teach or define above the invention claimed in claims 40-51 and are therefore rejected under Nakada in view of Asato for the same reasons set fourth in the rejection of claims 40-51, supra.

31. Specifically as to claim 28, Nakada taught a processor comprising a first execution unit (fig. 4, ALU1) having at least one first input (line from OP11 to ALU1) and a first output

(BPS1);

at least one second execution unit (ALU2) having at least one second input (line from OP21 to ALU2) and a second output (BPS2);

a first input register connected to said at least one first input (OP11);

a second input register (OP21);

a multiplexer (SEL21) having a first input from said first input register (RCPS1), a second input from said second input register (RCPS2) and an output to said at least one second execution unit (line from SEL21 through OP21 to ALU2).

32. Nakada did not teach a register decode value that specified program control over the bypassing of data. However, Asato taught a system whereby the instruction set of the processor defined register decode values (fig. 1, b1, b2, fig. 5, b1, b2, p1, p2) which were utilized to directly control bypassing functionality within Asato's system (col. 2 lines 47-58). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have modified Nakada's bypassing network to be controlled by register decode values contained in instructions as taught by Asato because Asato taught that placement of register decode values into the instructions for control of the bypassing network provided advantages of reduced hardware, shorter processor design cycles, and shorter design correctness verification cycles (col. 2 lines 53-62).

33. New claims 52-53, when dependent upon claim 9, are rejected under 35 USC § 103 as being unpatentable over Asato, U.S. patent 6,145,074, as applied to claims 36-37.

34. New claims 52-53, when dependent upon claim 46, are rejected under 35 USC § 103 as being unpatentable over Nakada, U.S. patent 5,638,526, in view of Asato, U.S. Patent 6,145,074, for the same reasoning presented in the rejection of claims 36-37 and 52-53 when dependent upon claim 9, supra.

35. Applicant's arguments filed January 28, 2003, paper number 14, have been fully considered but they are not deemed to be persuasive.

36. In the remarks, applicant argues in substance:

A) That: "[as to claims 1-21] Asato does not show Applicants' claimed invention relating to an instruction set ***'that specifies one of a first register decode value which defines source operand bypassing.***'" (pg. 12)

This is not found persuasive because as to claims 1-21, applicant's claims define two embodiments claimed in the alternative. The second alternative embodiment claimed by applicant's claims relates to result forwarding, which is taught by Asato as detailed in the rejection. Therefore, because an embodiment claimed by the claims is read upon by the art, the claims are anticipated.

37. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

38. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

39. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
June 25, 2003

Richard Ellis
Primary Examiner
Art Unit 2183